REMARKS

Applicants thank the Examiner for the thorough consideration given the present application.

Claims 1-10 and 12-37 are currently being prosecuted and are amended. Claims 1, 15, and 29 are independent.

Reconsideration of this application, as amended, is respectfully requested.

Drawings

The Applicants have not received a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, indicating whether the formal drawings have been approved by the Official Draftsperson. Clarification with the next official communication is respectfully requested.

Formalities

The paragraph bridging pages 3 and 4 of the specification and claims 1-10 and 12-37 are amended to correct obvious, inadvertent errors in spelling and syntax.

Rejections under 35 U.S.C. §102(b) and §103(a)

Claims 1-7, 9, 11-21, 23, 25-33, and 35-37 stand rejected under 35 U.S.C. §102(b) as being anticipated by ZAVRACKY et al., U.S. Patent No. 5,705,424; and claims 8, 10, 22, 24, and 34

stand rejected under 35 U.S.C. §103(a) as being unpatentable over ZAVRACKY et al. These rejections are respectfully traversed.

While not conceding the appropriateness of the rejections, but merely to advance prosecution of the present application, independent claim 1 is amended to recite a combination of steps in a method for manufacturing a thin film transistor panel, including forming a black matrix on a plurality of thin film structures.

As fully disclosed in the present application, e.g., in the paragraph at page 8, lines 7-19, and in FIG. 3, the black matrix 34 is a photo mask used in the step of etching the transparent insulator for exposing the transparent electrode 18.

It is respectfully submitted that the combination of method steps set forth in independent claim 1 is not anticipated by ZAVRACKY et al., and that this patent fails to teach anything about forming a black matrix on a plurality of thin film transistor structures.

It is asserted in the Office Action that the ZAVRACKY et al. patent, at column 8, line 45, teaches that element 500 is an "implied black matrix". The Applicants respectfully submit that this is not the case. As discussed on page 8 of the present specification, the black matrix 34 is a photo mask for blocking light-leakage that could possibly occur. By contrast, ZAVRACKY et

al.'s element 500 is merely a "color filter system on one side of the transfer substrate such as a glass substrate 500."

Accordingly, it is respectfully submitted that the combination of method steps set forth in independent claim 1 is not anticipated by the prior art of record, including ZAVRACKY et al.

Independent claims 15 and 29 also recite novel combinations of method steps not taught or suggested in the cited art.

As amended herein, claim 15 is directed to a method of manufacturing a thin film transistor panel having a combination of steps, including forming a plurality of transparent electrodes corresponding to a plurality of thin film transistor structures on a bottom surface of a transparent insulator. Full support for presently amended claim 15 can be found, e.g., at page 10, lines 3-8, of the specification and in FIG. 4J.

In rejecting claim 15, the Office Action contends that ZAVRACKY et al. discloses a transparent insulator 26 and transparent electrodes 250, shown in FIGS. 1D and 9E, respectively. However, a careful review of these drawings reveals that element 26 of ZAVRACKY et al. has no thin film transistor structures on a bottom surface thereof. As such, this reference cannot teach forming a plurality of transparent electrodes corresponding to a plurality of thin film transistor structures on

a bottom surface of a transparent insulator, as recited in presently amended claim 15.

Claim 29 is directed to method for manufacturing a thin film transistor panel having a combination of steps, including forming a planarization layer on thin film transistor structures and a pixel via, and forming a plurality of transparent electrodes corresponding to the thin film transistor structures on the planarization layer. Support for presently amended claim 29 can be found, e.g., at page 11, lines 11-20, of the specification and in FIGS. 5F and 5G.

In rejecting claim 29, the Office Action merely identifies certain passages of ZAVRACKY et al. that allegedly anticipate the present invention. After a thorough review, however, it is respectfully submitted that nowhere in the ZAVRACKY et al. patent is there any teaching of the above-noted key feature of presently amended claim 29. There is no disclosure in ZAVRACKY et al. of forming a planarization layer on thin film transistor structures and a pixel via, and forming a plurality of transparent electrodes corresponding to the thin film transistor structures on said planarization layer, although the word "planarization" does appear at column 7.

Accordingly, it is respectfully submitted that the combination of method steps set forth in independent claim 29 is

not anticipated by the prior art of record, including ZAVRACKY et al.

In view of the foregoing, it is respectfully submitted that ZAVRACKY et al. fails to anticipate or disclose the present invention, and reconsideration and withdrawal of the rejections are respectfully requested. Independent claims 1, 15, and 29 should be in condition for allowance. Regarding the dependent claims, including claims 8, 10, 22, 24, and 34 which stand rejected under 35 U.S.C. §103(a) as being unpatentable over ZAVRACKY et al., these claims should also be allowable due to their dependence, either directly or indirectly, on allowable independent claims, as well as for the additional limitations contained therein.

CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants, therefore, respectfully request that the Examiner reconsider the outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

However, in the event that any outstanding matters remain, the Examiner is invited to telephone Carl T. Thomsen (Reg. No. 50,786) at (703) 205-8000.

Pursuant to 37 C.F.R. §§1.17 and 1.136(a), Applicants respectfully petition for a two-month extension of time in which to file this reply. Attached is a check for the required fee of $400.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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MARKED-UP COPY OF AMENDMENTS

IN THE SPECIFICATION:

Please **amend the paragraph beginning on page 3, line 19,** and **ending on page 4, line 2,** as follows:

[Besides, before] Before bonding the transparent substrate in the invention, a black matrix can be formed on the thin film transistor structure layer. The black matrix [is to define] defines the transparent range of pixels on the thin film transistor panel and [mask] masks the portion of the thin film transistor panel that is most likely to incur light-leakage problems. The black matrix can also be a photo mask in the step of etching the [transparet] transparent insulator for exposing the transparent electrode. In this case, a back exposure process is used (expose from the transparent substrate side of the thin film transistor panel). A positive photo-resist on the bottom of the transparent insulator will be exposed without an additional photo mask. A subsequent photolithographic process can be performed to generate a suitable contact via on the transparent insulator. The contact via allows the transparent electrode to be exposed from the transparent insulator side of the thin film transistor panel. Hence, this traditionally

complicated process is simplified, and productivity is increased.

IN THE CLAIMS:

Please **cancel claim 11** without prejudice to or disclaimer of the subject matter contained therein.

Please **amend claims 1-10 and 12-37** as follows:

1. (Amended) A method for manufacturing a thin film transistor panel, comprising at least[, comprises] the following [step] steps:

[provide] providing a silicon substrate;

[form] forming a [of] transparent insulator on [the] a front surface of said silicon substrate;

[form] forming a plurality of thin film transistor structures and a plurality of corresponding transparent electrodes on said transparent insulator;

forming a black matrix on said plurality of thin film transistor structures;

[bond] bonding a transparent substrate onto the front surface of said silicon substrate;

[remove] removing said silicon substrate; and

[etch] etching said transparent insulator to expose said plurality of corresponding transparent [electrode] electrodes.

2. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein said transparent insulator is SiO_x.

3. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein said transparent insulator is SiN_x.

4. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein the thickness of said transparent insulator is [below one] less than 1 micrometer.

5. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein [the material of] said transparent electrode is made of indium tin oxide.

6. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein said transparent substrate is a glass substrate.

7. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein said transparent substrate is a polymer substrate.

8. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein the [method for] step of removing said silicon substrate includes chemical mechanical polishing.

9. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein [said] the [method for] step of removing said silicon substrate includes an etching process.

10. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, further [comprises a step for] comprising forming an alignment mark on said transparent insulator.

12. (Amended) A method for manufacturing a thin film transistor panel of claim **1**, wherein the step [for] of forming said plurality of thin film transistor [structure] structures and said plurality of corresponding transparent [electrode] electrodes further comprises:

[form] forming a transistor film and a transparent electrode on said transparent insulator;

[form] forming a gate insulator covering said transistor thin film and said transparent electrode;

[form] forming a gate electrode on said gate insulator corresponding to [the] a position of said transistor thin film;

[form] forming an interlayer on said gate electrode and said gate insulator;

[form] forming a metal contact layer on said gate insulator; and

[form] forming a passivation layer on said metal contact layer.

13. (Amended) A method for manufacturing a thin film transistor panel of claim **12**, wherein the [material of said] transistor thin film [can be anyone of] is selected from the group consisting of polycrystal silicon(p-Si), polycrystal germanium (p-Ge), polycrystal silicon germanium (p-SiGe), crystal silicon (c-Si), crystal germanium (c-Ge), and crystal silicon germanium (c-SiGe).

14. (Amended) A method for manufacturing a thin film transistor panel of claim **12**, further [comprises a step of] comprising forming a color filter on said passivation layer.

15. (Amended) A method for manufacturing a thin film transistor panel, comprising at [lease, comprise] least the following steps:

[provide] providing a silicon substrate;

[form] forming a transparent insulator on [the] a front surface of said silicon substrate;

[form] forming a plurality of thin film transistor structures on said [the] transparent insulator;

[bond] bonding a transparent substrate onto the front surface of said silicon substrate;

[remove] removing said silicon substrate; and

[form] forming a plurality of transparent electrodes corresponding to said plurality of thin film transistor [structure] structures on [the] a bottom surface of said transparent insulator.

16. (Amended) A method for forming a thin film transistor panel of claim **15**, wherein said transparent insulator is SiO_x.

17. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein said transparent insulator is SiN_x.

18. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein the thickness of said transparent insulator is [below one] less than 1 micrometer.

19. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein [the material of] said transparent electrode is made of indium tin oxide.

20. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein said transparent substrate is a glass substrate.

21. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein said transparent substrate is a polymer substrate.

22. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein the [method for] step of removing said silicon substrate includes chemical mechanical polishing.

23. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein [said] the [method for] step of removing said silicon substrate includes an etching process.

24. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, further [comprises a step for] comprising forming an alignment mark on said transparent insulator.

25. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, further [comprises a step for] comprising forming a [back] black matrix on said plurality of thin film transistor [structure] structures before bonding said transparent substrate onto the front surface of said silicon substrate.

26. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, wherein the step [for] of forming said plurality of thin film transistor [structure] structures and said plurality of corresponding transparent [electrode] electrodes further comprises:

[form] forming a transistor thin film on said front surface of said transparent insulator;

[form] forming a gate insulator covering said transistor thin film and said plurality of transparent [electrode] electrodes;

[form] forming a gate electrode on said gate insulator corresponding to [the] a position of said transistor thin film;

[form] forming an interlayer on said gate electrode and said gate insulator;

[form] forming a metal contact layer on said gate insulator; and

[form] forming a passivation layer on said metal contact layer.

27. (Amended) A method for manufacturing a thin film transistor panel of claim **26**, wherein [the material of] said transistor thin film [can be anyone of] is selected from the group consisting of polycrystal silicon(p-Si), polycrystal germanium (p-Ge), polycrystal silicon germanium (p-SiGe), crystal silicon (c-Si), crystal germanium (c-Ge), and crystal silicon germanium (c-SiGe).

28. (Amended) A method for manufacturing a thin film transistor panel of claim **15**, further [comprises a step of] comprising forming a color filter on the bottom surface of said transparent insulator before forming said transparent electrode.

29. (Amended) A method for manufacturing thin film transistor panel, comprising at least[, comprises] the following [step] steps:

[provide] providing a silicon substrate;

[bond] bonding a transparent substrate onto [the] a back surface of said silicon substrate;

[reduce] reducing the thickness of said silicon substrate to form a layer of crystal silicon thin film;

[form] forming a plurality of thin film transistor structures on said crystal silicon thin film;

[etch] etching said thin film transistor [structure layer] structures and said crystal silicon thin film to form a suitable pixel via;

[form] forming a planarization layer on said thin film transistor [structure] structures and said pixel via; and

[form] forming a plurality of transparent electrodes corresponding to the thin film transistor structures on said planarization layer.

30. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein the thickness of said transparent insulator is [below one] less than 1 micrometer.

31. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein [the material of] said transparent electrode is made of indium tin oxide.

32. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein said transparent substrate is a glass substrate.

33. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein said transparent substrate is a polymer substrate.

34. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein the [method for] step of removing said silicon substrate includes chemical mechanical polishing.

35. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein [said] the [method for] step of removing said silicon substrate includes an etching process.

36. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein the [method for] step of forming said thin film transistor [structure comprise] structures further comprises:

[form] forming a source region and a drain region on said crystal silicon thin film;

[form] forming a gate insulator covering said transistor thin film and said transparent electrode;

[form] forming a gate electrode on said gate insulator;

[form a] forming an interlayer on said gate electrode and said gate insulator; and

[form] forming a metal contact layer on said gate insulator.

37. (Amended) A method for manufacturing a thin film transistor panel of claim **29**, wherein the planarization layer is also a color filter.